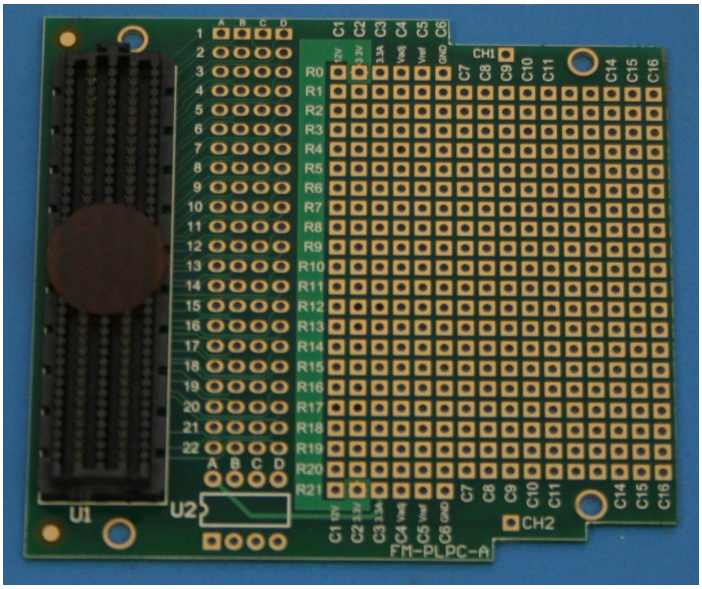
FM-PLPC Prototype Development Platform

Development platform for FPGA Mezzanine Card Low Pin count functions

Features

- Industry standard, modular FPGA I/O in an FPGA Mezzanine Card (FMC, aka VITA 57), module
- FMC Compliant (when cut as marked) with standard mounting holes and connector
- Breakout of Low Pin count Connector (LPC) pins to 0.1” development matrix
- Standard FMC outline or extended length option
- Extended Ground rails and Power breakout for two power connections
- Control signals available for user connections in development matrix
- On board EEPROM footprint for configuration management and user data

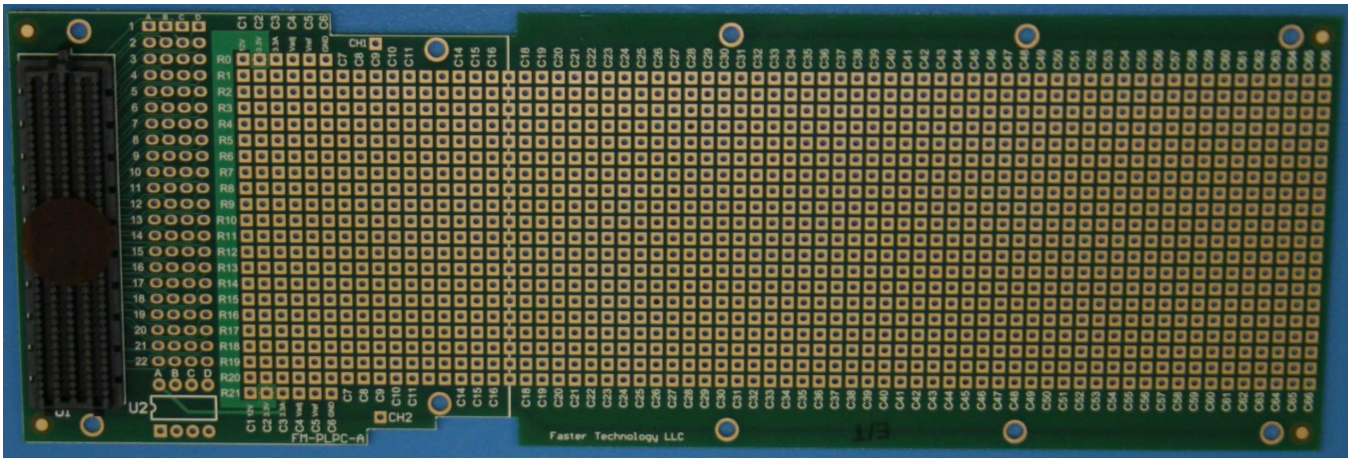


Benefits

- Provides rapid means to develop new FMC functions
- Extended length version enables development of more complex FMC systems for later integration to standard FMC form factor
- Footprint for on board EEPROM simplifies complete FMC compatible interface
- Breakout of High Speed serial interfaces, clocks and control signals enables easy completion of full capability FMC functions

Description

The FM-PLPC breaks out the complete LA bank of signals from the standard FMC Low Pin count Connector and the standard power rail and control signals. The user can add standard 0.1 inch spaced components and sockets for a wide variety of active and passive devices. The extended length version offers almost four times the prototype area of the standard length version to enable development of very complex capabilities. Standard control signals are available for the user to complete the interface to the chosen carrier card.



Faster Technology LLC
1812 Avenue D, Suite 202 Katy, TX 77493 T: 281.391.5482 F: 281.391.9384 info@fastertechnology.com

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FM-PLPC Technical Specifications

LPC Connections	
LA00 through LA33 P and N to development matrix connections	
High Speed serial lines	DP0_M2C and DP0_C2M breakout adjacent to LPC connector
Development Matrix	
Standard 0.1 inch hole matrix	
Optional customer cut to standard length FMC	20 X 16 hole matrix
Extended length option	20 X 66 hole matrix
Reference Clocks	
GBTCLK0_M2C	Breakout adjacent to LPC connector
CLK0_M2C and CLK1_M2C	Breakout adjacent to LPC connector
Power connections	
Power lines in development matrix	Two rows in development matrix—user connection to power Two GND rows in development matrix
JTAG	
Standard signals available in development matrix	
TDI tied to TDO with user removable link	
Supported Host boards	
Virtex-6	Xilinx EK-V6-ML605-G
Kintex-7	Xilinx EK-K7-KC705
On-board serial EEPROM footprint	
EEPROM interface	I^2C via FMC SCL / SDA interface I^2C address via FMC GA0 / GA1 Write Protect from footprint to development matrix
Miscellaneous	
FMC compliance	ANSI/VITA 57.1 (February 2010) compliant when cut as marked
V_{ADJ}	User determined
Power Good - PG_C2M	Available to user in development matrix
Module Present - PRESENT_M2C	Grounded with user removable link and available in development matrix

Related Products

FM-S14	FMC compliant module with one quad SFP/SFP+ cage supporting up to four (4) SFP or SFP+ Modules
FM-S18	FMC compatible module with two quad SFP/SFP+ cages to support up to eight (8) SFP or SFP+ Modules
FM-S28	FMC compatible module with two QSFP/ QSFP+ cages to support up to two (2) QSFP or QSFP+ Modules

Ordering Information

FM-PLPC-E	Extended length FMC development platform

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